OFP-CW31QG-FR4CL

400G 2km OSFP Optical Transceiver

Features

- **OSFP MSA compliant**
- **4 CWDM lanes MUX/DEMUX design**
- **100G Lambda MSA 400G-FR4 Specification compliant**
- **Up to 2km transmission on single mode fiber (SMF) with FEC**
- **Operating case temperature: 0 to 70℃**
- **8x53.125Gb/s electrical interface (400GAUI-8)**
- **Data Rate 106.25Gbps (PAM4) per channel.**
- **Maximum power consumption 12W**
- **Duplex LC connector**
- **RoHS compliant**

Applications

- **Data Center Interconnect**
- **400G Ethernet**
- **Infiniband interconnects**
- **Enterprise networking**

General Description

This product is a 400Gb/s Octal Small Form-factor Pluggable (OSFP) optical module designed for 2km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals, and multiplexes them into a single channel for 400Gb/s optical transmission. Reversely, on the receiver side, the module optically de- multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals, and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 76-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 2km fiber transmission

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the OSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Functional Description

The module incorporates 4 independent channels on CWDM4 1271/1291/1311/1331nm center wavelength, operating at 100G per channel. The transmitter path incorporates a quad channel EML driver and EML lasers together with an optical multiplexer. On the receiver path, an optical de- multiplexer is coupled to a 4 channel photodiode array. A DSP basis gearbox is used to convert 8 channels of 25GBaud PAM4 signals into 4 channels of 50GBaud PAM4 signals and also an 8-channel retimer and FEC block are integrated in this DSP. The electrical interface is compliant with IEEE 802.3bs and OSFP MSA in the transmitting and receiving directions, and the optical interface is compliant to IEEE 802.3bs with duplex LC

connector.

A single +3.3V power supply is required to power up this product. As per MSA specifications the module offers 4 low speed hardware control pins: SCL, SDA, INT/RSTn and LPWn/PRSn

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value can be
2.2k ohms to 4.7k ohms.

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host. The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 1 shows these 3 zones.

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host. The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 1 shows these 3 zones.

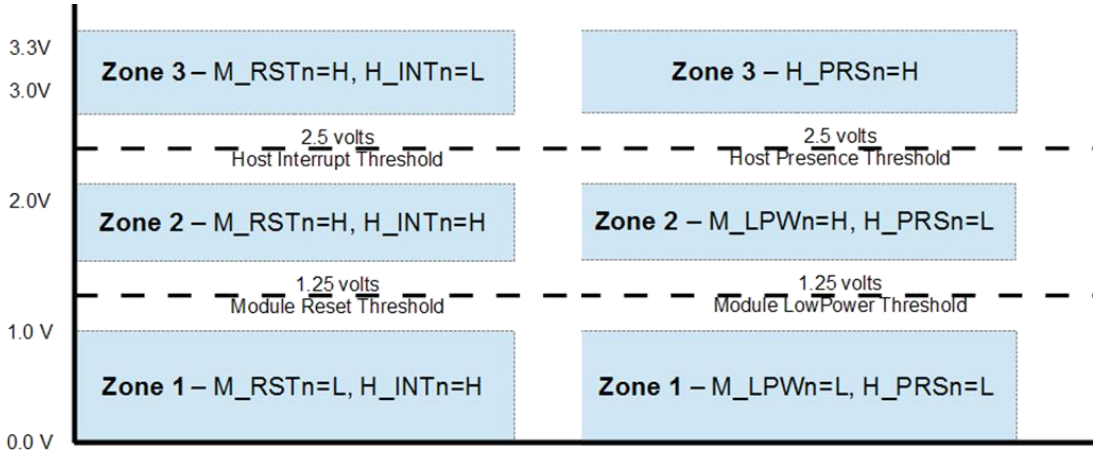


Figure 1. Voltage Zones

Transceiver Block Diagram

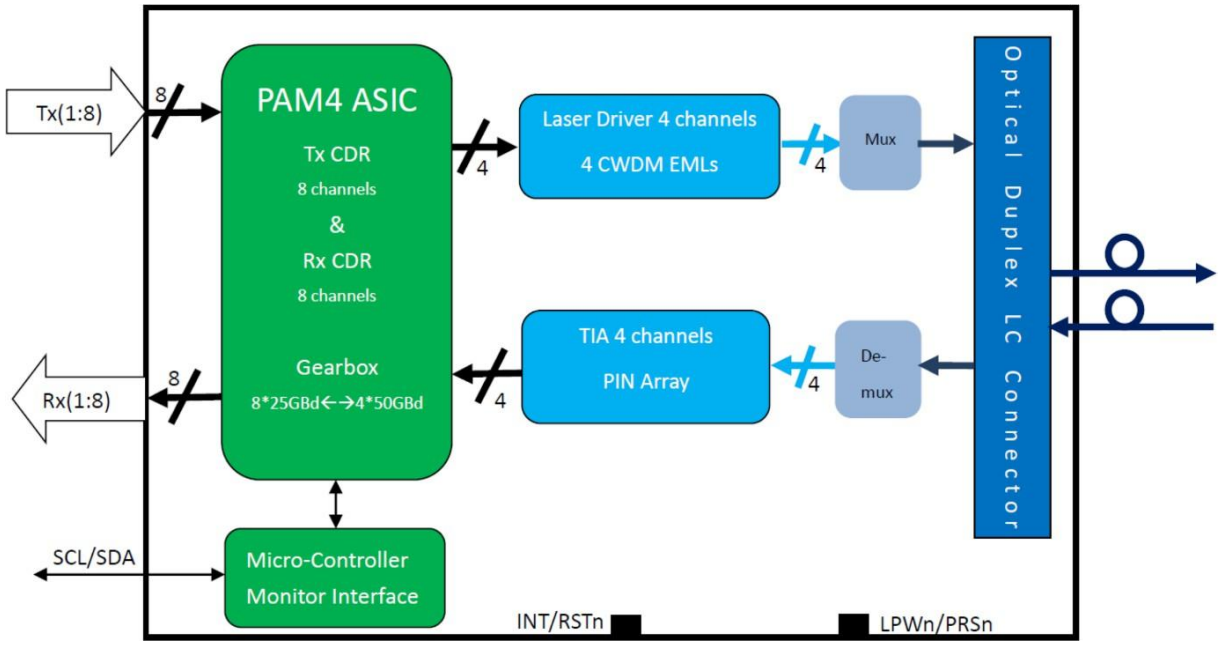


Figure 2. Transceiver Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	0	70	degC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

Recommended

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	D	0.5		2000	m	2

Notes:

1.FEC provided by host system.

2.FEC required on host system to support maximum distance.

Electrical Characteristics

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				12	W	
Supply Current	Icc			3.64	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	

Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each Lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:：

1.With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

2.Meets BER specified in IEEE 802.3bs 120E.1.1.

3.DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

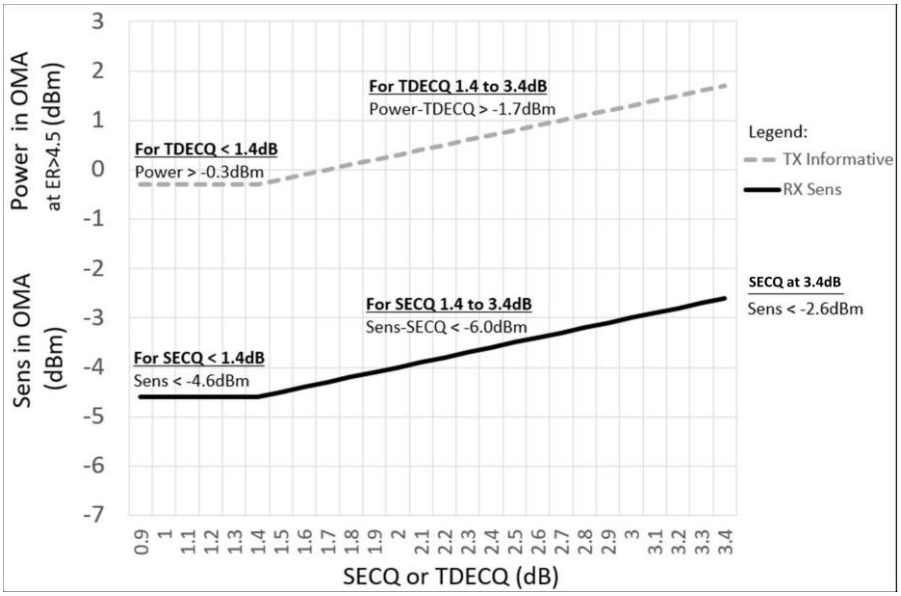
Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter						
Data Rate, each Lane		53.125 ±100 ppm			GBd	
Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30			dB	Modulated
Total Average Launch Power	P_T			9.3	dBm	
Average Launch Power, each Lane	P_{AVG}	-3.3		3.5	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	-0.3		3.7	dBm	2
Launch Power in OMA_{outer} minus TDECQ, each Lane		-1.7			dB	For ER ≥4.5dB
Launch Power in OMA_{outer} minus TDECQ, each Lane		-1.6			dB	For ER <4.5dB
Transmitter and Dispersion Eye Clouser for PAM4, each Lane	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5			dB	
Difference in Launch Power between any Two Lanes (OMA_{outer})				4	dB	
$RIN_{17.1}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			17.1	dB	
Transmitter Reflectance	T_R			-26	dB	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-20	dBm	
Receiver						
Data Rate, each Lane		53.125 ±100 ppm			GBd	
Modulation Format		PAM4				

Damage Threshold, each Lane	TH_d	4.5			dBm	3
Average Receive Power, each Lane		-7.3		3.5	dBm	4
Receive Power (OMA_{outer}), each Lane				3.7	dBm	
Difference in Receiver Power between any Two Lanes (OMA_{outer})				4.1	dB	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			-5.0	dBm	For BER of 2.4E-4
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS	See Figure 5			dBm	5
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-30			dBm	
LOS De-assert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 6)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test		0.9		3.4	dB	
OMA_{outer} of each Aggressor Lane			1.5		dBm	

Notes:
1.Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2.Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMA_{outer} (min) must exceed the minimum value specified here.
3.The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
4.Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5.Measured with conformance test signal for BER = $2.4x10^{-4}$. A compliant receiver shall have stressed receiver sensitivity (OMA_{outer}), each lane values below the mask of Figure 4, for SECQ values between 0.9 and 3.4 dB.

These test conditions are for measuring stressed receiver sensitivity.They are not characteristics of the receiver.

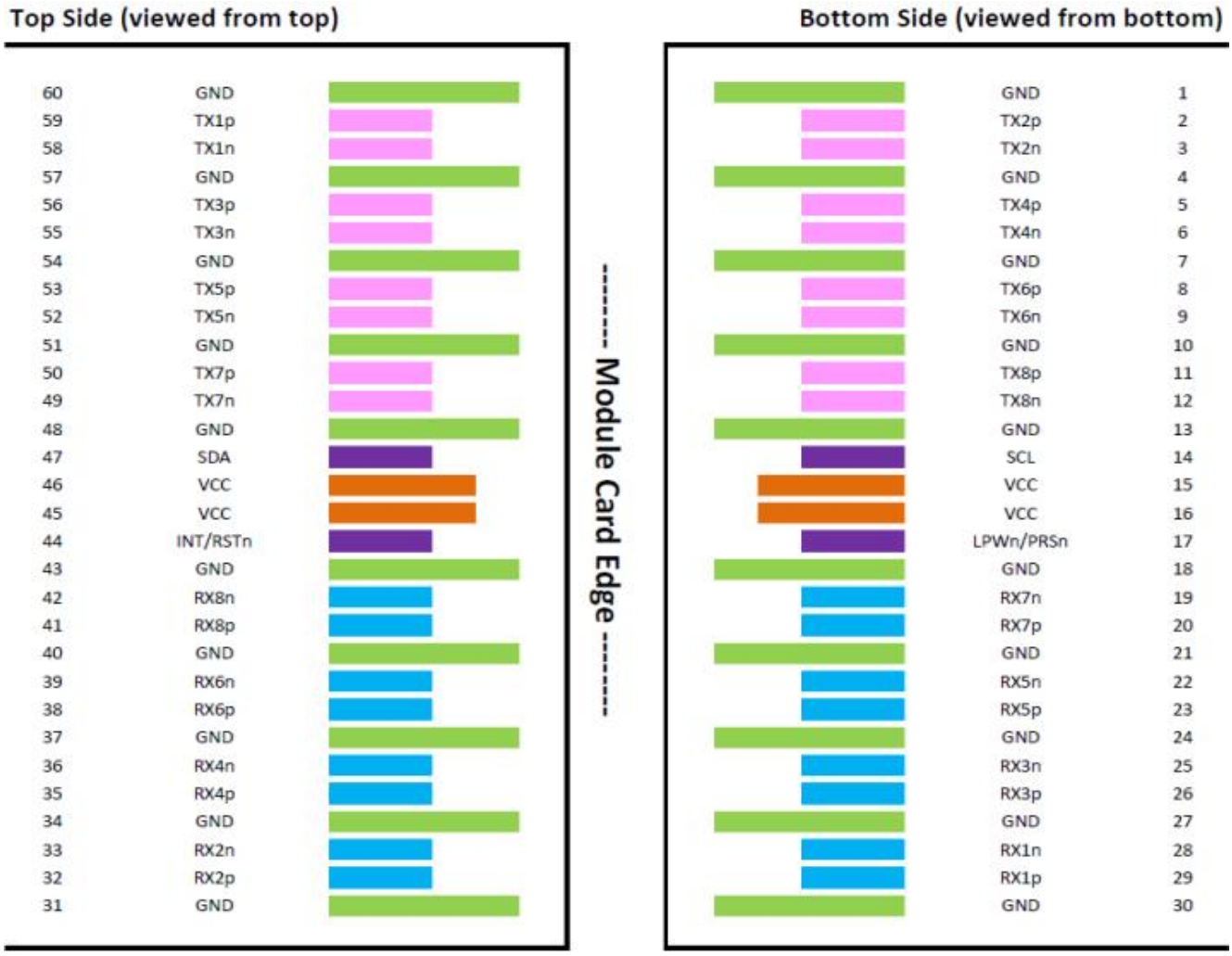


Digital Diagnostic Functions

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:
1.Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Pin Assignment and Description



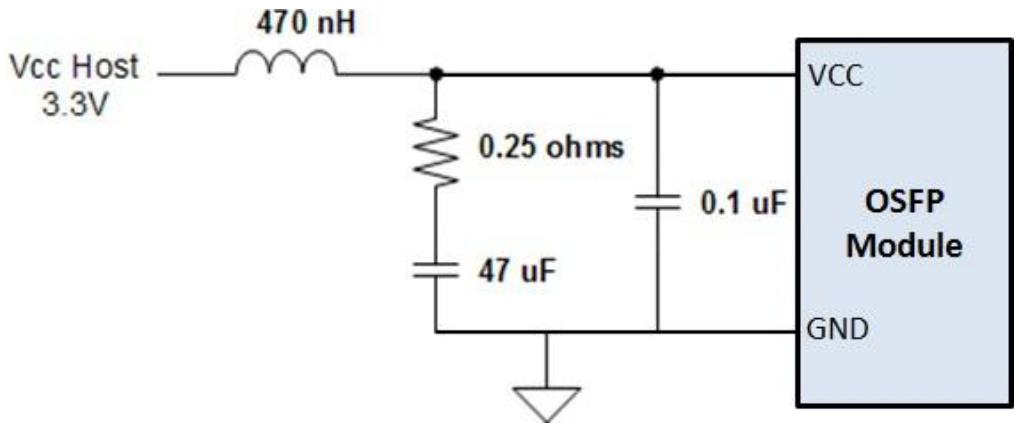
Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2p	Transmitter Data Non-Inverted	3	
3	CML-I	Tx2n	Transmitter Data Inverted	3	
4		GND	Ground	1	1
5	CML-I	Tx4p	Transmitter Data Non-Inverted	3	
6	CML-I	Tx4n	Transmitter Data Inverted	3	

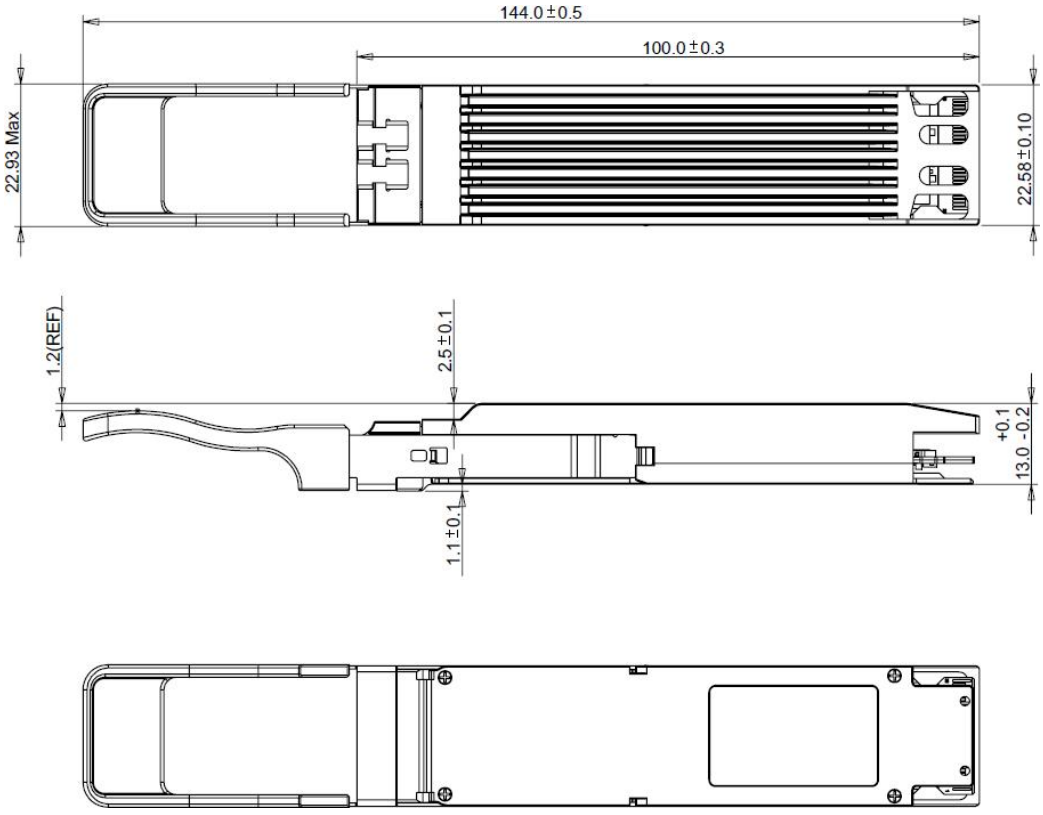
7		GND	Ground	1	1
8	CML-I	Tx6p	Transmitter Data Non-Inverted	3	
9	CML-I	Tx6n	Transmitter Data Inverted	3	
10		GND	Ground	1	1
11	CML-I	Tx8p	Transmitter Data Non-Inverted	3	
12	CML-I	Tx8n	Transmitter Data Inverted	3	
13		GND	Ground	1	1
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	3	2
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present	3	
18		GND	Ground	1	1
19	CML-O	Rx7n	Receiver Data Inverted	3	
20	CML-O	Rx7p	Receiver Data Non-Inverted	3	
21		GND	Ground	1	1
22	CML-O	Rx5n	Receiver Data Inverted	3	
23	CML-O	Rx5p	Receiver Data Non-Inverted	3	
24		GND	Ground	1	1
25	CML-O	Rx3n	Receiver Data Inverted	3	
26	CML-O	Rx3p	Receiver Data Non-Inverted	3	
27		GND	Ground	1	1
28	CML-O	Rx1n	Receiver Data Inverted	3	
29	CML-O	Rx1p	Receiver Data Non-Inverted	3	
30		GND	Ground	1	1
31		GND	Ground	1	1
32	CML-O	Rx2p	Receiver Data Non-Inverted	3	
33	CML-O	Rx2n	Receiver Data Inverted	3	
34		GND	Ground	1	1
35	CML-O	Rx4p	Receiver Data Non-Inverted	3	

36	CML-O	Rx4n	Receiver Data Inverted	3	
37		GND	Ground	1	1
38	CML-O	Rx6p	Receiver Data Non-Inverted	3	
39	CML-O	Rx6n	Receiver Data Inverted	3	
40		GND	Ground	1	1
41	CML-O	Rx8p	Receiver Data Non-Inverted	3	
42	CML-O	Rx8n	Receiver Data Inverted	3	
43		GND	Ground	1	1
44	Multi-Level	INT/RSTn	Module input/Module Reset	3	
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVCMOS-I/O	SCL	2-wire Serial interface Data	3	2
48		GND	Ground	1	1
49	CML-I	Tx7n	Transmitter Data Inverted	3	
50	CML-I	Tx7p	Transmitter Data Non-Inverted	3	
51		GND	Ground	1	1
52	CML-I	Tx5n	Transmitter Data Inverted	3	
53	CML-I	Tx5p	Transmitter Data Non-Inverted	3	
54		GND	Ground	1	1
55	CML-I	Tx3n	Transmitter Data Inverted	3	
56	CML-I	Tx3p	Transmitter Data Non-Inverted	3	
57		GND	Ground	1	1
58	CML-I	Tx1n	Transmitter Data Inverted	3	
59	CML-I	Tx1p	Transmitter Data Non-Inverted	3	
60		GND	Ground	1	1
1: OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module and all module voltages are referenced to this potential unless otherwise noted.					
2: Open-Drain with pull up resistor on Host.					

Recommended Power Supply Filter



Mechanical Dimensions



Ordering information

Part Number	Product Description
OFP-CW31QG-FR4CL	400Gbps, OSFP FR4 , 1271-1331nm, 2km, 0°C~+70°C

For More Information

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