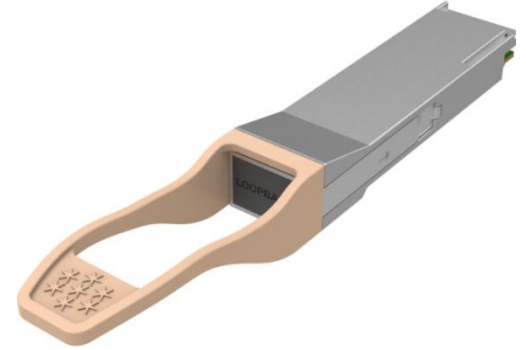


QFP-LPHG 100G QSFP28 Active Electrical Loopback Module

Features

- Hot-pluggable QSFP28 form factor
- 4 channels Electrical Loopback Module
- Supports 103.125Gb/s aggregate bit rates
- Low power dissipation <2.5W
- RoHS compliant (lead-free)
- Single 3.3V power supply
- QSFP MSA compliant
- Commercial case temperature range of 0°C to 70°C



Applications

- 100G Ethernet

Description

QFP-LPHG QSFP28 active electrical loopback is used for testing 100G QSFP28 transceiver ports in board level test. By substituting for a full-featured QSFP28 transceiver, the electrical loopback provides a cost effective low loss method for QSFP28 port testing.

The QFP-LPHG is packaged in a standard MSA housing compatible with all QSFP28 ports. Transmit data from the host is electrically routed (internal to the loopback module) to the receive data outputs and back to the host. Since the loopback module does not contain laser diodes, photodiodes, laser driver or transimpedance amplifier chips, etc., it provides an economical way to exercise QSFP28 ports during R&D validation, production testing and field testing.

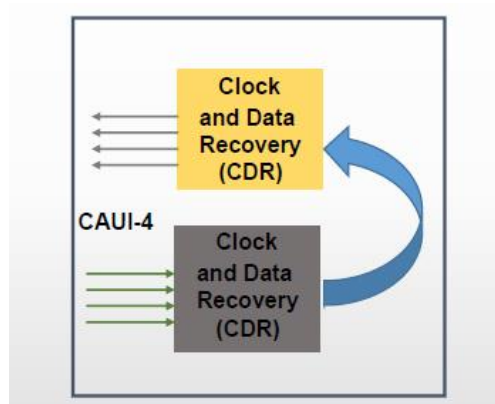


Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	$V_{cc}+0.3$	V
Storage Temperature	T_s	-40	85	°C
Case Operating Temperature	T_c	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case Temperature	T_c	0		70	°C
Data Rate Per Lane	fd		25.78125		Gb/s
Humidity	Rh	5		85	%
Power Dissipation	P_m			2.5	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude	ΔV_{in}	300		1100	mVpp
Differential Output Voltage Amplitude	ΔV_{out}	300		900	mVpp
Bit Error Rate	BER			E-12	
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	$V_{cc}-0.5$		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground ^{Note5}
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground ^{Note5}
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground ^{Note5}
8	LVTTL-I	MODSEIL	Module Select ^{Note6}
9	LVTTL-I	ResetL	Module Reset ^{Note6}
10		VCCRx	+3.3V Receiver Power Supply
11	LVC MOS-I	SCL	2-wire Serial interface clock ^{Note6}
12	LVC MOS-I/O	SDA	2-wire Serial interface data ^{Note6}
13		GND	Module Ground ^{Note5}
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground ^{Note5}
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground ^{Note5}
20		GND	Module Ground ^{Note5}

21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground ^{Note5}
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground ^{Note5}
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board ²
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode ^{Note6}
32		GND	Module Ground ^{Note5}
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground ^{Note5}
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground ^{Note5}

Note:

Note5. Module circuit ground is isolated from module chassis ground within the module.

Note6. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

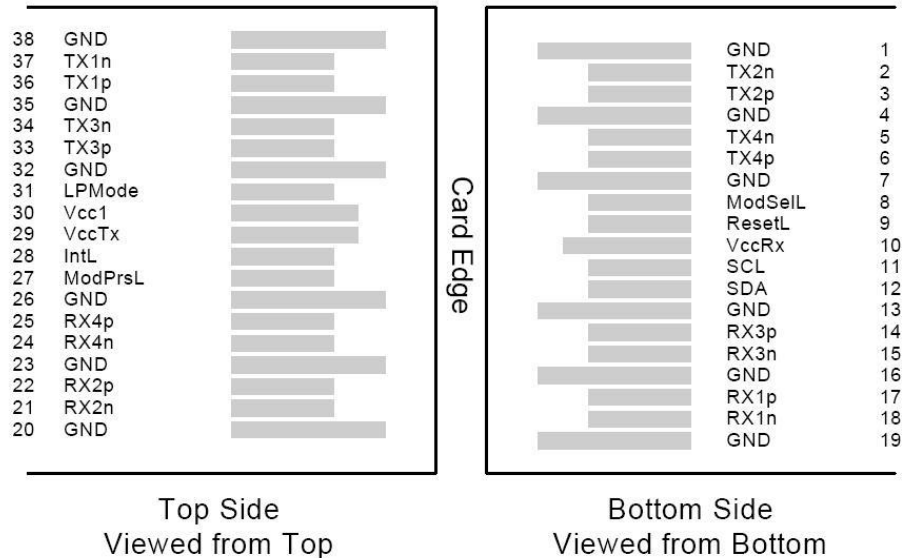


Figure 2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length ($t_{\text{Reset_init}}$) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_{init}) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_{init}) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

QSFP28 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure 3.

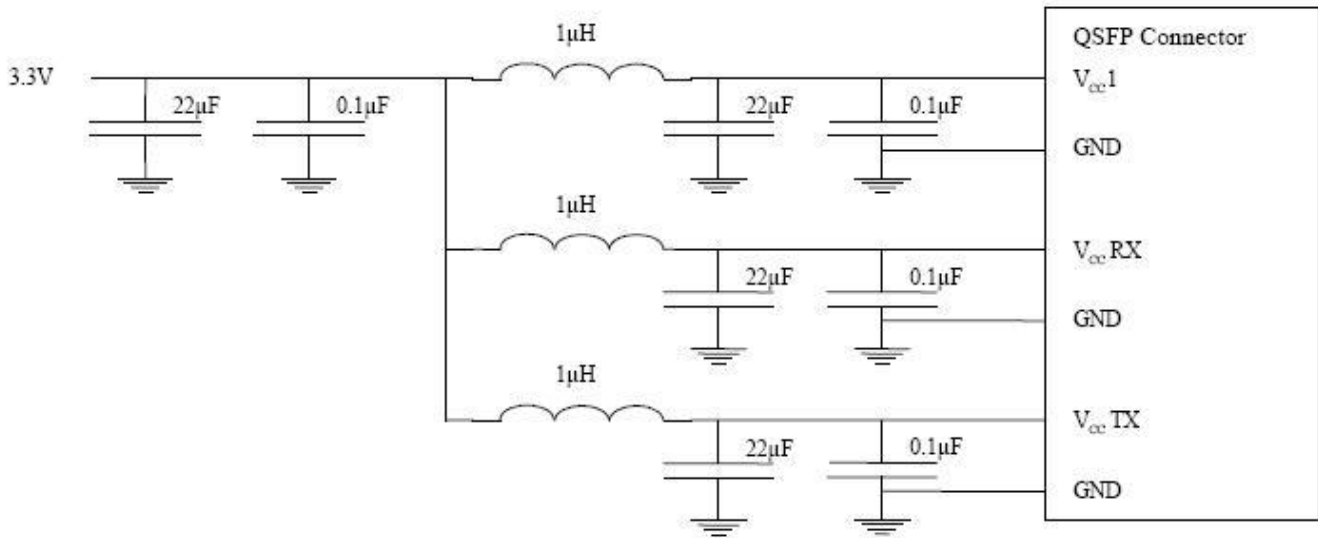


Figure 3. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Fibertop QSFP28 Loopback Module. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 4. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

2-wire serial address, 1010000x (A0h)"

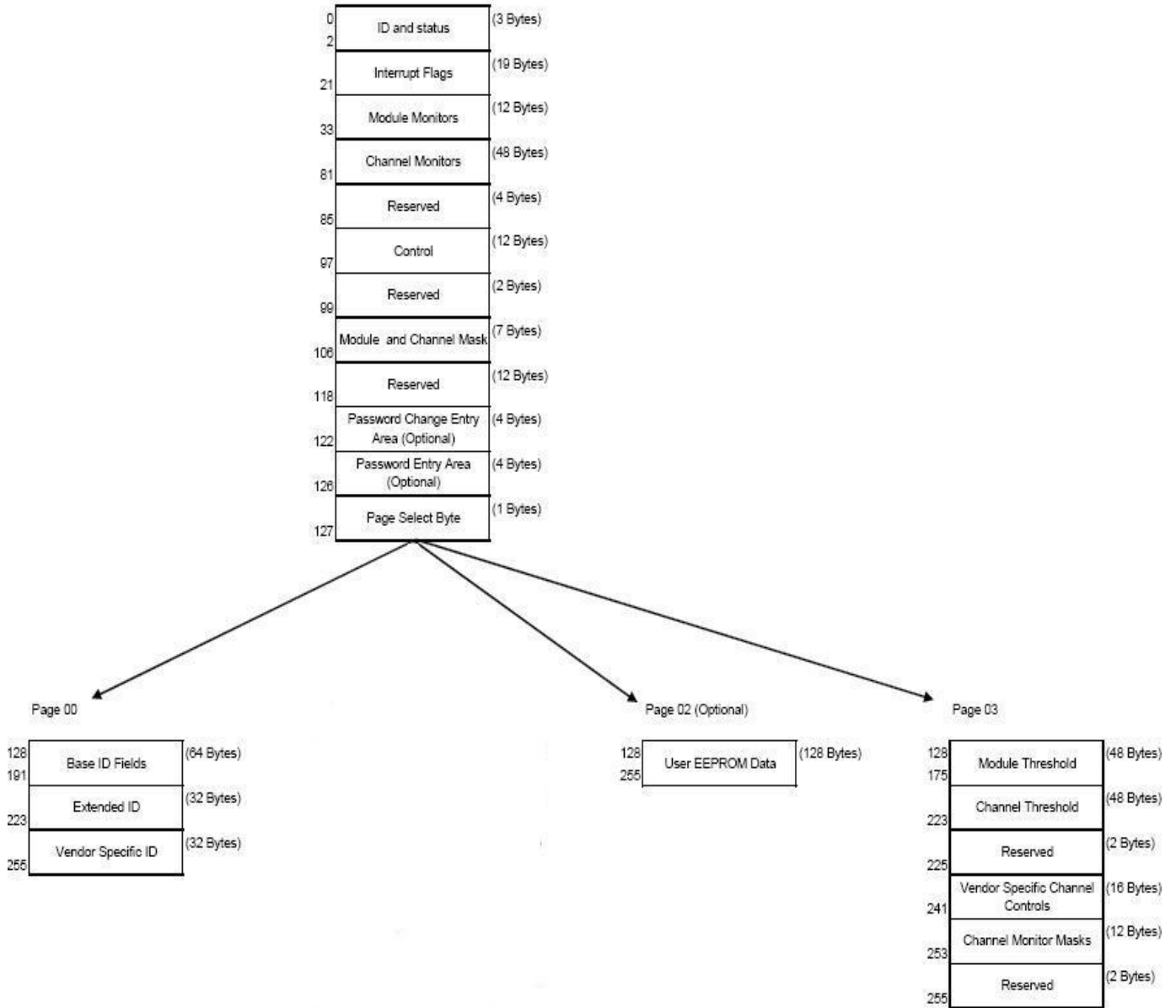


Figure 4. QSFP Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure5.Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure6.Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μ m (1 Byte)	Link length supported for EBW 50/125 μ m fiber, units of 2 m
144	Length 50 μ m (1 Byte)	Link length supported for 50/125 μ m fiber, units of 1 m
145	Length 62.5 μ m (1 Byte)	Link length supported for 62.5/125 μ m fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand [†]
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure7.Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and page00.page03 upper memory please see SFF-8436 document.

Mechanical Dimensions

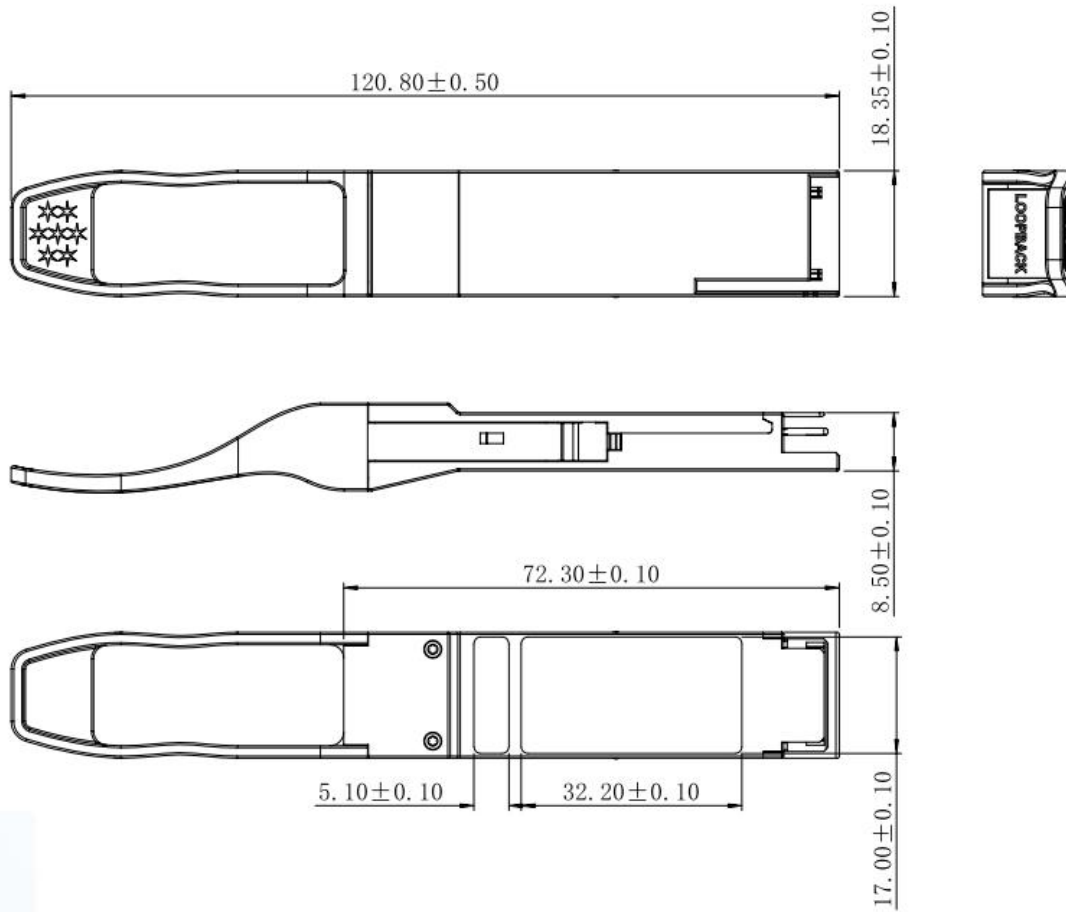


Figure 8. Mechanical Specifications

Ordering information

Part Number	Product Description
QFP-LPHG	100G QSFP28 Active Electrical Loopback

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