

## QFP-LW31HD-40DC

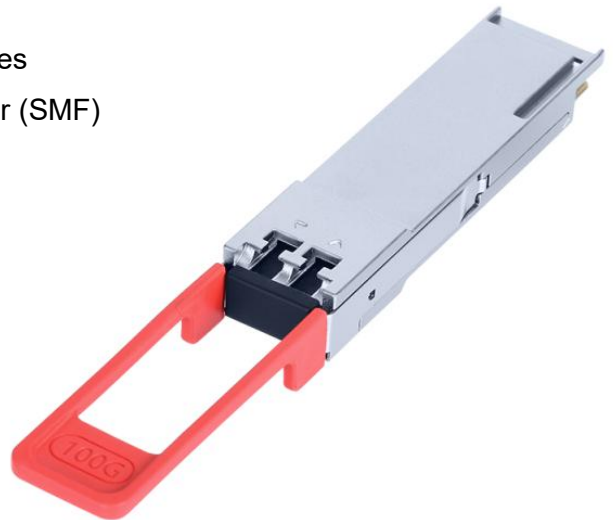
100Gbps QSFP28 Transceiver, Single Mode, 40km Reach

### DESCRIPTION

QFP-LW31HG-40DC is Multi-rate 100Gb/s QSFP28 ER4 transceiver. It is compliant with the QSFP28 MSA and IEEE 802.3ba and OTU4 411-9D1F. QSFP28 ER4 transceiver modules are designed for use in 100 Gigabit Ethernet and 4x28G OTN client interfaces over single mode fiber.

### FEATURES

- Hot-pluggable QSFP28 form factor
- Supports 103.1Gb/s and 112Gb/s aggregate bit rates
- Maximum link length of 40km on Single Mode Fiber (SMF)
- Power dissipation < 5W
- Built-in digital diagnostic functions
- Built-in CDR
- 4x28Gb/s DFB-based LAN-WDM transmitter
- Duplex LC receptacles
- Single 3.3V power supply
- RoHS compliant
- Operating case temperature: 0~+70°C



### APPLICATION

- 100GBASE-ER4 100G Ethernet
- 100GE 4WDM-40 Applications
- OTN OTU4 411-9D1F

### ABSOLUTE MAXIMUM RATINGS (TC=25°C, UNLESS OTHERWISE NOTED)

Module performance is not guaranteed beyond the operating range.  
Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	Ts	-40	-	+85	°C	
Maximum Supply Voltage	Vcc	-0.3	-	3.6	V	
Operating Relative Humidity	RH	15	-	+85	%	

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Data Rate	DR	25.78		27.95	Gb/s	1
Operating Case Temperature	Tcase	0		70	°C	
Fiber Length on SMF	L			40	km	With FEC

Notes:

1. Supports 100GBASE-ER4 per IEEE 802.3ba and OTU4 411-9D1F per ITU-T G.959.1.

## PIN DESCRIPTIONS

Pin	Symbol	Name/Description	Ref.
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3 V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1

20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	2
29	Vcc Tx	+3.3 V Power supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMODE	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

1. Circuit ground is internally isolated from chassis ground.

2. IntL is an open collector/drain output, which should be pulled up with a 4.7k – 10k Ohms resistor on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

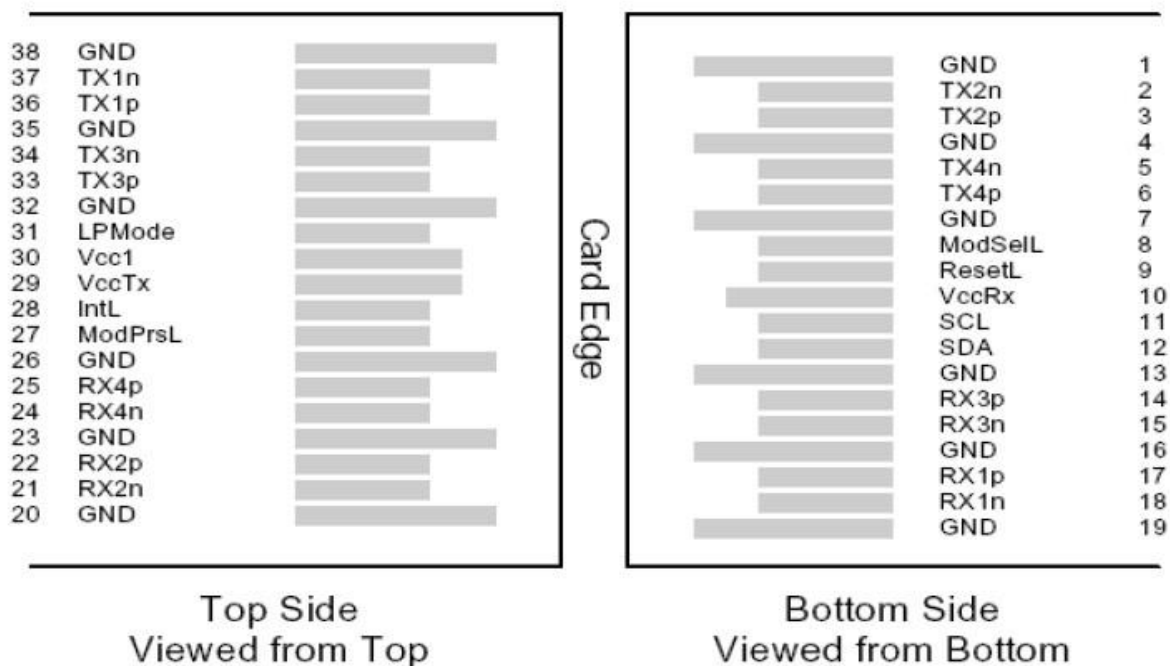


Figure 1 – QSFP28-Compliant 38-Pin Connector (Per SFF-8679)

## ELECTRICAL SPECIFICATION

Parameter	Symbol	Min	Typical	Max	Units	Notes
Supply Voltage	Vcc	3.135		3.465	V	
Supply Current	Icc			1.5	A	
Module Total Power	P			5	W	1
<b>Transmitter</b>						
Signaling rate per lane		25.78		27.95	Gb/s	
Differential input impedance	Zin		100		Ohm	
Differential input voltage amplitude	Vin			900	mVp-p	
<b>Receiver</b>						
Signaling rate per lane		25.78		27.95	Gb/s	
Differential Output impedance	Zout		100		Ohm	
Differential output voltage amplitude	Vout	400		900	mVp-p	
Eye width		0.57			UI	
Vertical eye closure				5.5	dB	
Transition time, 20% to 80%	Tr/Tf	12			ps	

Notes:

- Maximum total power value is specified across the full temperature and voltage range.

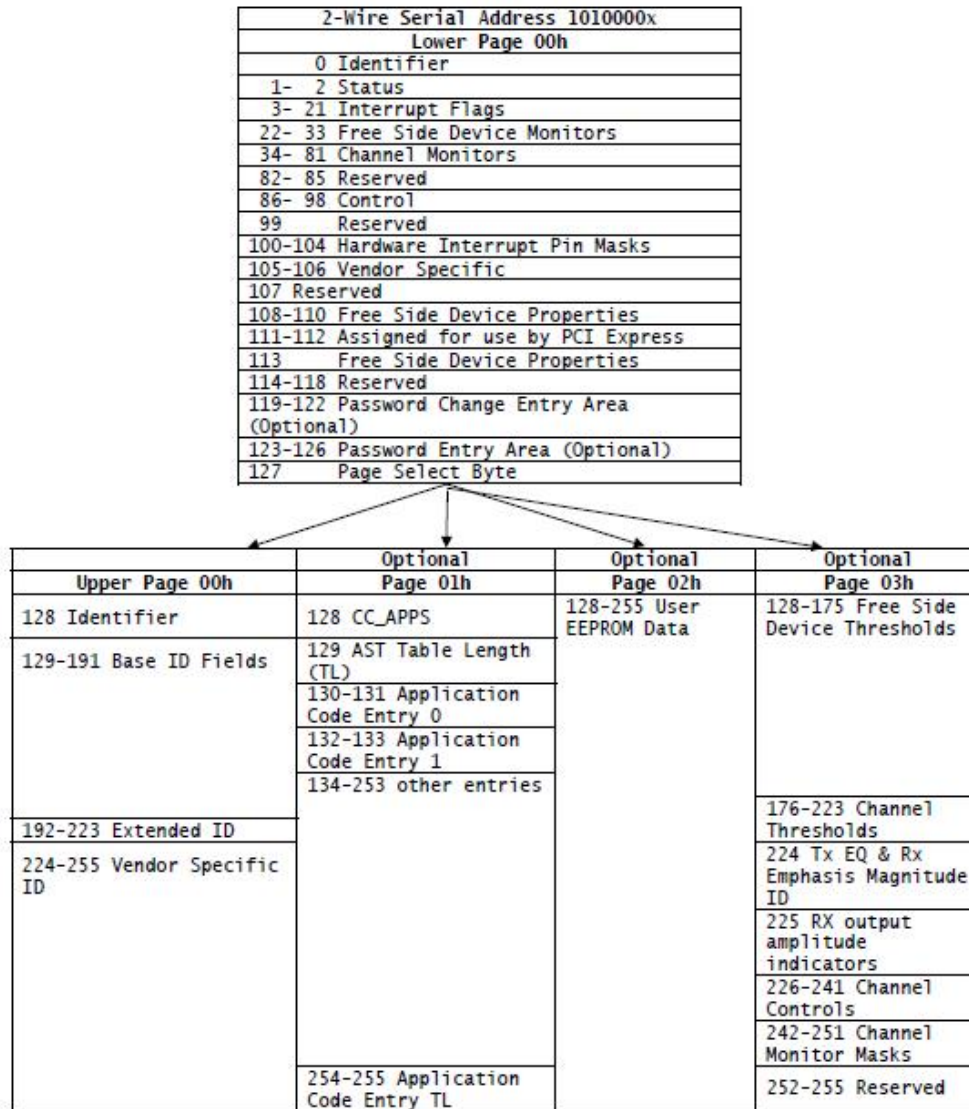
## OPTICAL SPECIFICATION

Parameter	Symbol	Min	Typical	Max	Units	Notes
<b>Transmitter</b>						
Signaling rate per lane		25.78125±100ppm 27.9525± 20 ppm			Gb/s	1
Center wavelength	$\lambda$	1294.53 – 1296.59 1299.02 – 1301.09 1303.54 – 1305.63 1308.09 – 1310.19			nm	
Sidemode Suppression ratio	SMSR	30			nm	
Transmit OMA per Lane	TXP	0.5		6.5	dBm	
Transmit Average Power per Lane	Pout	-2.5		6.5	dBm	
Optical Extinction Ratio	ER	4			dB	
Average launch power of OFF transmitter, per lane				-30	dBm	
Optical return loss tolerance	RL			20	dB	
Relative Intensity Noise	RIN			-130	dB/Hz	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				2
<b>Receiver</b>						
Signaling rate per lane		25.78125±100ppm 27.9525± 20 ppm			Gb/s	1
Center wavelength	$\lambda$	1294.53 – 1296.59 1299.02 – 1301.09 1303.54 – 1305.63 1308.09 – 1310.19			nm	
Average Receive Power per Lane	RXP	-20		-4	dBm	3,4
		-18		-4		3,5
Receive Power (OMA) per Lane	RxOMA			-3.5	dBm	
Receive Sensitivity in OMA, each Lane	SEN			-18.5	dBm	4
				-16.5		5
Receiver Reflectance	Rfl			-26	dB	
LOS De-Assert	LOSD			-23	dBm	
LOS Assert	LOSA	-35			dBm	
LOS Hysteresis	LOSh	0.5			dB	

Notes:

1. Transmitter and Receiver consists of 4 lasers and photodiode operating at 25.78Gb/s each for 100GBASE-ER4,
2. Hit ratio 5E-5.
3. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. Measured with a PRBS 231-1 test pattern @25.78Gbps, BER ≤5E-5.
5. Measured with a PRBS 231-1 test pattern @27.95Gbps, BER ≤1E-6

## DIGITAL DIAGNOSTIC FUNCTIONS



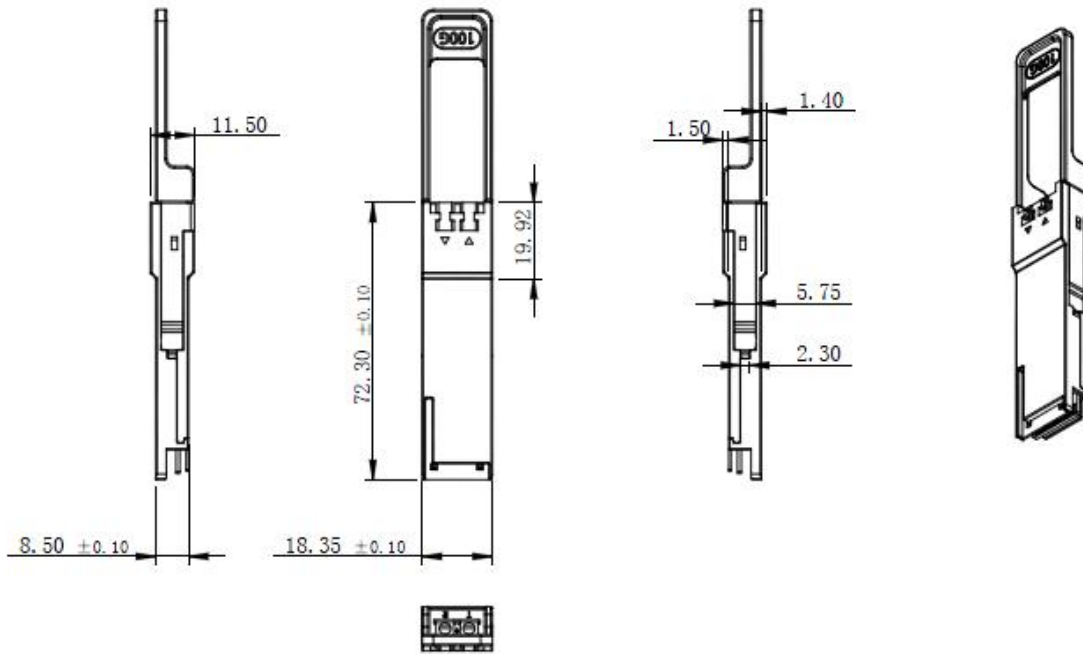
**Figure 2 – Two-Wire Interface Fields**

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. The 2-wire serial interface shall consist of a master and slave. The fixed side shall be the master and the free side shall be the slave. Control and data are transferred serially. The master shall initiate all data transfers. Data can be transferred from the master to the slave and from the slave to the master. The 2-wire interface shall consist of

clock (SCL) and data (SDA) signals. The master utilizes SCL to clock data and control information on the 2-wire bus. The master and slave shall latch the state of SDA on the positive transitioning edge of SCL. The SDA signal is bi-directional. During data transfer, the SDA signal shall transition when SCL is low. A transition on the SDA signal while SCL is high shall indicate a stop or start condition. For more information, please see the QSFP28 MSA documentation.

## MECHANICAL SPECIFICATIONS

Unit:mm



## Ordering information

Part Number	Product Description
QFP-LW31HD-40DC	Multi-rate 100Gbps QSFP28 ER4, LC, 40km, 0°C~+70°C, with DDM

## For More Information

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